

EMI/EMC SIMULATION: THIRD PARTY SERVICE

ANALYSIS BEFORE PROTOTYPING

SILVANO CHIALINA



EXONX SRL

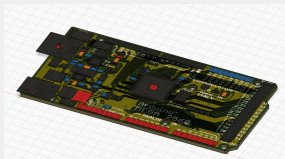
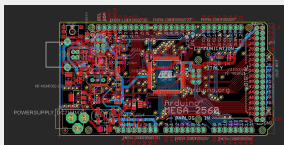
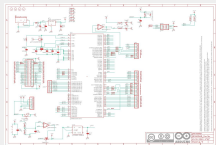
VIA JACOPO LINUSSIO 1, 33020 AMARO (UD) - ITALY

22TH 03 2023

SIMULATION SETUP

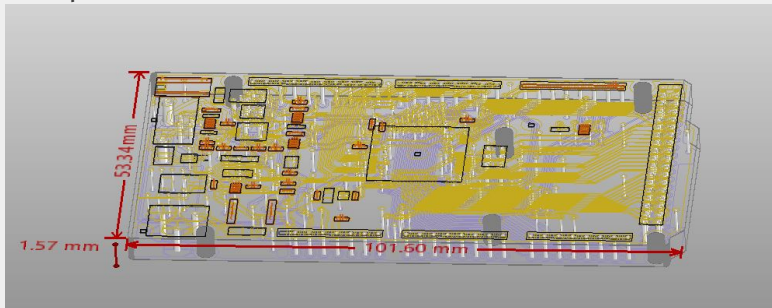
PROJECT IMPORT

The CAD project composed of Schematic, PCB and CAM files is imported into the simulator. The preferred format are: IPC 2581, ODB++, Metor, GDSI, Ansys, Gerber



PROJECT IMPORT

At the end of the process the project is incorporated in 3D into the simulator with all the relevant characteristics of the PCB and the components



EMI ANALYSIS

DESIGN ROULES CHECK

The project is analyzed by verifying if the design rules are respected

EMI Scan Violations (EMI Scan Sim 1)

- Power/Ground Trace = GND, Layer = top, Segment Width = 0.2794, Violating Segment = [[19.689, 31.619] [20.0124, 31.2956]]
- Power/Ground Trace = GND, Layer = top, Segment Width = 0.3048, Violating Segment = [[40.934, 30.419] [41.5663, 29.8709]]
- Power/Ground Trace = GND, Layer = top, Segment Width = 0.254, Violating Segment = [[54.8132, 36.2458] [54.8132, 35.4076]]
- Power/Ground Trace = GND, Layer = top, Segment Width = 0.2794, Violating Segment = [[47.3, 20.3464] [47.3, 21.3017]]
- Power/Ground Trace = GND, Layer = top, Segment Width = 0.3048, Violating Segment = [[81.32, 37.23] [82.0071, 37.23]]
- Power/Ground Trace = GND, Layer = top, Segment Width = 0.2032, Violating Segment = [[47.9919, 21.4655] [47.8028, 21.2344]]
- Power/Ground Trace = GND, Layer = top, Segment Width = 0.2032, Violating Segment = [[47.8028, 21.2344] [47.8028, 19.4818]]
- Power/Ground Trace = USBVCC, Layer = top, Segment Width = 0.254, Violating Segment = [[17.489, 33.548] [15.895, 33.548]]
- Power/Ground Trace = USBVCC, Layer = top, Segment Width = 0.254, Violating Segment = [[15.895, 33.548] [15.113, 32.766]]
- Power/Ground Trace = USBVCC, Layer = top, Segment Width = 0.254, Violating Segment = [[15.113, 32.766] [15.113, 32.004]]
- Power/Ground Trace = USBVCC, Layer = top, Segment Width = 0.254, Violating Segment = [[15.113, 32.004] [14.4121, 31.3031]]

Decoupling

- Decoupling Capacitor Density
- Decoupling Capacitor Distance from IC Power Pin

IC Power/Ground-Reference Pin Distance to Via

- IC Pin = IC7.6, Layer Name = top, Message = No Via(s) Found in Search Box, Net Name = A.307
- Associated Via = [15.24, 30.353], Distance = 4.25804, IC Pin = IC4.32, Layer Name = top, Message = Pin to Via to Plane Distance Exceeds Limit, Net Name = GND
- IC Pin = IC4.31, Layer Name = top, Message = No Via(s) Found in Search Box, Net Name = USBVCC
- IC Pin = IC4.28, Layer Name = top, Message = No Via(s) Found in Search Box, Net Name = GND
- IC Pin = IC4.3, Layer Name = top, Message = No Via(s) Found in Search Box, Net Name = GND
- IC Pin = IC4.4, Layer Name = top, Message = No Via(s) Found in Search Box, Net Name = GND
- IC Pin = IC3.32, Layer Name = top, Message = No Via(s) Found in Search Box, Net Name = GND
- IC Pin = IC3.80, Layer Name = top, Message = No Via(s) Found in Search Box, Net Name = GND

Decoupling Capacitor Distance to Via

- Associated Via = [36.1, 2.54], Box = [[35.9998, 5.292] [39.4382, 8.932]], Cap Pin = C4.1, Capacitor = C4, Distance = 4.64412, Message = Distance Exceeded, Net = GND
- Associated Via = No Via, Box = [[56.4214, 37.55] [59.8596, 41.19]], Cap Pin = C5.1, Capacitor = C5, Distance = No Distance, Message = No Via Within Limit, Net = GND

Power/Ground-Reference Trace Decoupling

Power Via Density

Disparate Reference Overlay

- Layer 1 = top, Layer 2 = bottom, Net 1 = USBVCC, Net 2 = GND, Overlap Area = 6.45527, Violation Box = [[2.745, 23.77] [6.145, 25.67]]
- Layer 1 = top, Layer 2 = bottom, Net 1 = XVCC, Net 2 = GND, Overlap Area = 6.45527, Violation Box = [[2.745, 27.67] [6.145, 29.57]]

[Decoupling] - [IC Power/Ground-Reference Pin Distance to Via]
The trace connecting between the IC power or ground-reference pin and the associated via to the power/ground-reference plane must be no longer than the specified distance.

Units: mm

Sort Violations By: Severity Name

Expand All Collapse All

Select nets cited in checked violations

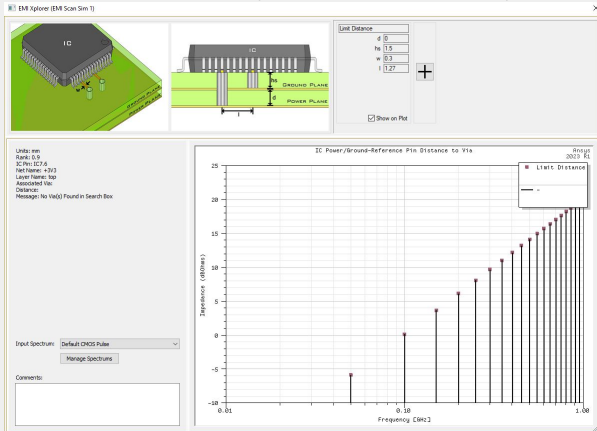
Showing violations of severity: 0 to 1

EMI Explorer

Close

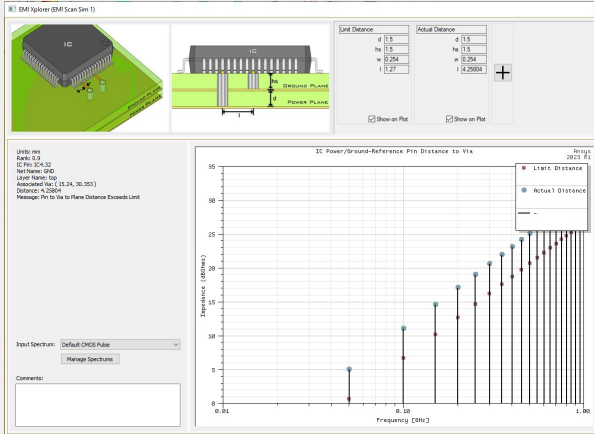
DESIGN ROULES CHECK

Details of rule violations are provided, for example:



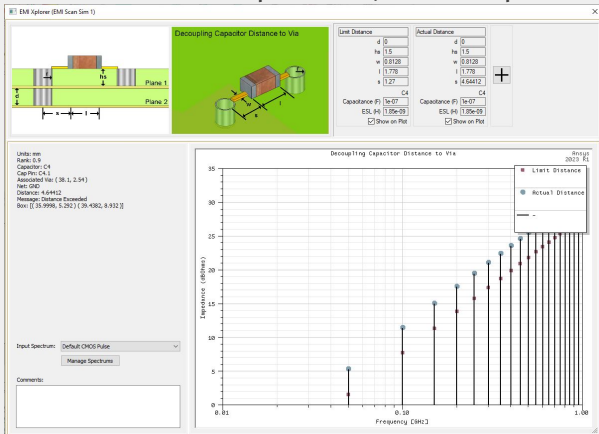
DESIGN ROULES CHECK

Details of rule violations are provided, for example:



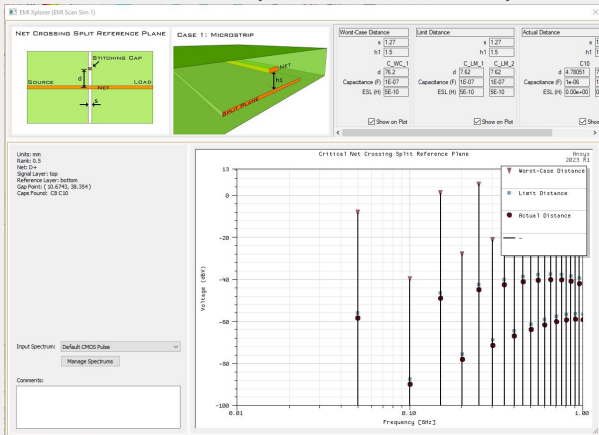
DESIGN ROULES CHECK

Details of rule violations are provided, for example:



DESIGN ROULES CHECK

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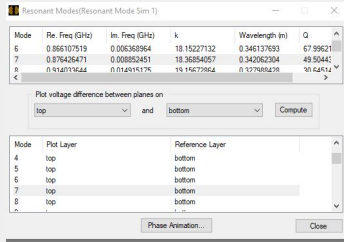
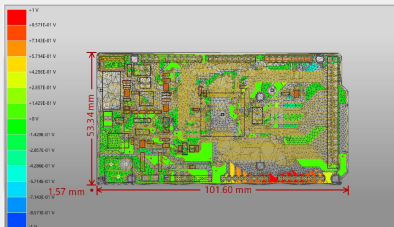
The report provided will contain the breakdown of individual violations with an indication of the location where it occurred. Based on this output it is possible to update the PCB in order to reduce the probability of having a critical behavior from an EMC point of view.

RESONANCES

The resonance analysis allows to verify any areas of the PCB that could amplify the emissions and the effects of the RF immunity. Also this analysis can be done before the realization of the prototypes in order to limit the areas and/or the resonance effects.

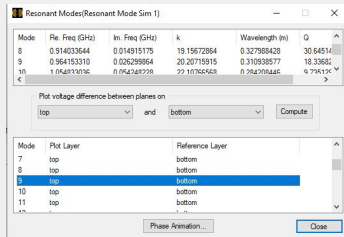
RESONANCES

In this example we see une area closed to the connector



RESONANCES

In this example we see one area closed to one component



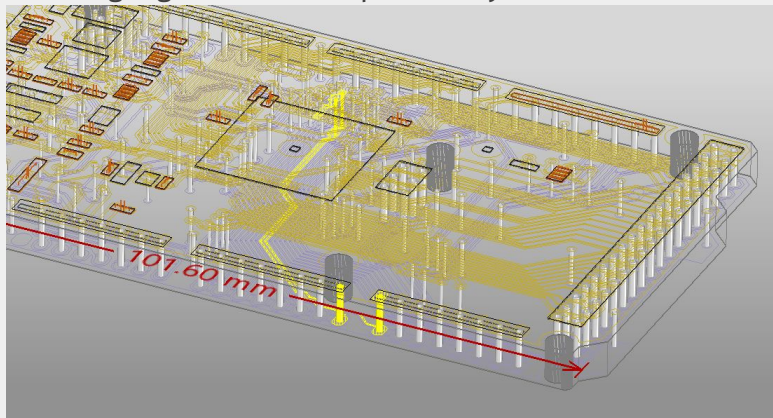
INTERFERENCE ANALYSIS

INTERFERENCE ANALYSIS

In critical areas it is possible to make an accurate analysis of the effect of immunity to electromagnetic fields. Interference testing is done for various field orientations and over a very wide frequency range..

INTERFERENCE ANALYSIS

Here are highlighted two nets potentially at risk



INTERFERENCE ANALYSIS

Induced field

Compute Induced Voltage

Simulation name: Induced Voltage Sim 1

Frequency Range Setup

	Start Freq	Stop Freq	Num. Points	Distribution
1	200MHz	1GHz	50	By Decade

Add Above Add Below Delete Selection Preview...

Save Load Set Default Clear Default

Single Incidence

Spherical

Incidence: Phi: 0 degrees Theta: 90 degrees

Polarization E0: E0_Phi: 0 E0_Theta: 1

Cartesian

Incidence: X: -1 Y: 0 Z: 0

Polarization E0: X: 0 Y: 0 Z: -1

Multiple Incidence (Spherical)

Incidence

Phi		Theta	
Start:	0 degrees	Start:	0 degrees
Stop:	270 degrees	Stop:	180 degrees
Step size:	90	Step size:	90

Polarization E0: E0_Phi: 0 E0_Theta: 1

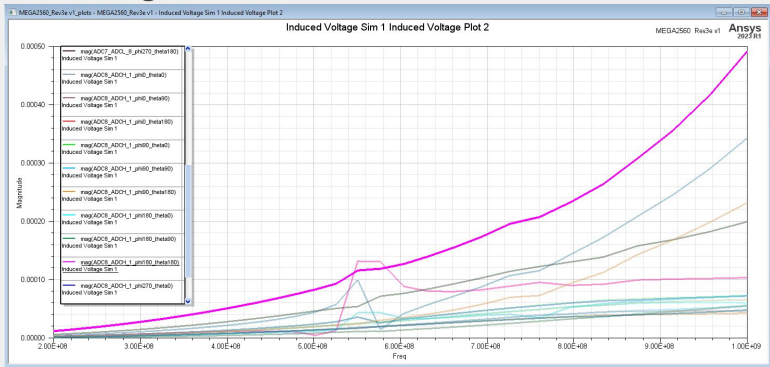
Save voltage at port locations for all angles

Magnitude of normalized Polarization E0: 1 Center Vector Visualization

Other solver options... Save Settings Launch Close

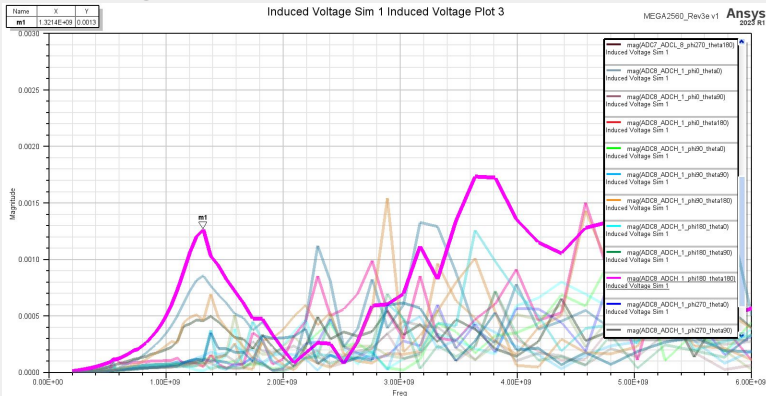
INTERFERENCE ANALYSIS

Induced voltage



INTERFERENCE ANALYSIS

Induced voltage



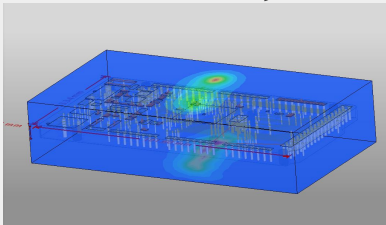
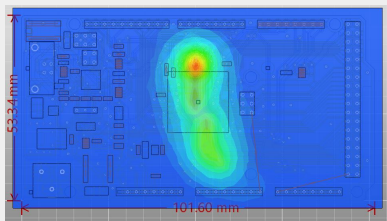
RADIATED EMISSION

The near field and radiated field analysis is done by stressing the areas of the PCB that can radiate the most. Below are the results of the near-field simulations and the results of the radiated field.

RADIATED EMISSION

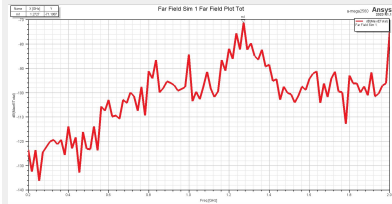
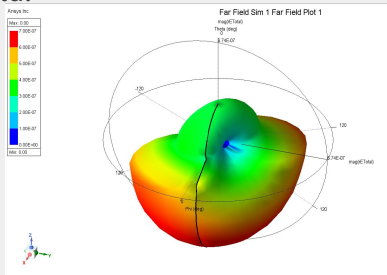
Near field calculated from 1 to 1.4GHz

This result is calculated at 1.3GHz. The emission is asymmetrical



RADIATED EMISSION

It is possible to calculate the radiated field, in this case at 1m. You can see the representation in polar coordinates and the evaluation of the total field. The peak is at 1.27GHz, it corresponds to the peak of the voltage induced by the radiated field.



REFERENCES



SUSAN C. HAGNESS ALLEN TAFLONE.

COMPUTATIONAL ELECTRODYNAMICS

THE FINITE-DIFFERENCE TIME-DOMINE METHOS. - THIRD EDITION.

Artech House, 2005.

NOTES